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III. Remarks

A. Rejection under 35 U.S.C. §102(e)

The Action rejects Claims 1-2, 6-7, 13-14, 17-19 and 21-22 as being anticipated by U.S. Patent Application Publication No. 2004/0051120A1 to Kato. Reconsideration of this rejection is respectfully requested in view of the following arguments.

1. Kato does not teach a gate "confined to be substantially within the active region of the transistor device"

In rejecting Claim 1, the Examiner states that the gate 7 of the transistor device of Kato is "configured to be substantially within the active region of the device." (Final Rejection, Page 3, Lines 1-2). In the Response to Arguments section, the Examiner states that the "claimed invention does not say anything about the gate not extending beyond the active region." Reconsideration of this point is respectfully requested.

Claim 1 does not recite, as set forth in the Action, that the gate is "configured" to be substantially within the active region of the device. Rather, Claim 1 recites that the gate is "**confined**" to be substantially within the active region of the device. The term "confined" is generally understood as meaning "to hold within a location" or "to keep within limits." (Merriam-Webster OnLine Dictionary) (www.m-w.com). Clearly, therefore, by reciting that the gate is "confined to be substantially within the active region of the device," the claimed MOS device includes a gate that is limited (i.e., "does not extend beyond," to use the Examiner's phrasing) to be substantially within the active region of the device.

Applicants again direct the examiner to the attached Exhibit which includes an annotated copy of FIGS. 1(a) and 1(b) of Kato. From this illustration, it can be seen that the dimension of the Kato gate that is defined substantially parallel to the width of the device (labeled "W" in FIG. 1(a)) is not **confined** to be substantially within the active region 14 of the device. Indeed, it appears that a very large portion of gate element 7, perhaps around 40% of the total width W of the gate 7, extends beyond the active region 14 of the device. Therefore, it cannot be said that

the width of the gate 7 of Kato is "**confined** to be substantially within the active region of the device."

As Kato does not teach this feature, Claim 1 is not anticipated by the cited reference. For analogous reasons, independent Claims 14 and 21 are also not anticipated by Kato. Therefore, it is submitted that Claims 1, 14 and 21 and the claims that depend therefrom are allowable over the art of record.

2. Kato does not teach an "isolation structure" that "substantially isolate[s] one or more portions of the first source/drain region from corresponding portions of the second source drain region"

a. Amendment to Claim 1

Claim 1 has been amended to recite that the "metal-oxide-semiconductor device" is a "transistor device" and that the first and second source/drain regions are part of the "transistor device." It is submitted that one of ordinary skill would have understood that this claim, even prior to the amendments, recited features of a discrete transistor device. One of ordinary skill would understand that by reciting a "MOS device" that has the recited first and second laterally spaced source/drain regions, gate and the defined "length" and "width" as claimed in claim 1 prior to amendment, the claimed MOS device is an MOS transistor device. These amendments, therefore, do not narrow the claims nor raise new issues for consideration and search.

From the foregoing, it follows that the components recited in Claim 1 (e.g., source/drain regions, gate, etc.) are part of a single transistor device. Therefore, as discussed below, it is improper to select features from different transistor devices of Kato formed in a substrate for purposes of rejecting the claims.

b. Argument

Claim 1 recites that the transistor device includes "an isolation structure formed in the semiconductor layer, the isolation structure being configured to substantially isolate one or more portions of the first source/drain region from corresponding portions of the second source/drain regions." Claim 1 makes clear that this isolation structure is formed to isolate source/drain

regions **of the same MOS device**, not of different MOS devices. This point is emphasized in Claim 1 by the recitation that the source/drain regions are part of the "transistor" device, i.e., they are first and second source/drain regions of a single transistor device.

The Examiner relies on isolation structure 24 for providing this feature and concludes that the "isolation structure 24 is formed to isolate source/drain regions of the same device on substrate 27." Any source/drain regions isolated by isolation structure 24 may be formed on the save device substrate, but they are not part of the same MOS device as claimed and as would be understood by those in the art, and clearly are not part of the same MOS transistor device.

With reference to FIG. 1(b), Kato clearly shows that isolation structures 24 are formed in between adjacent devices, not in between portions of the first and second source/drain regions of a single transistor device. Indeed, Paragraph 49 of Kato cited by the Examiner expressly states that "[e]ach of the **element regions 14 can be in contact with the metallic layer 13, while being separately insulated from one another** in a lateral direction by insulating layer 24." (emphasis added) The top plan view of FIG. 1(a) does not show regions 24, though it is submitted that it appears from the figures that isolation regions 24 will surround active regions 14 and not isolate portions of first and second source/drain regions 17 of a transistor device formed therein.

For these additional reasons, it is submitted that Claim 1 is not anticipated by Kato. Accordingly, it is submitted that Claim 1 and the claims which depend therefrom are allowable over Kato.

Independent Claims 14 and 21 also recite the gate, source/drain and isolation structure features discussed above in connection with independent Claim 1. Though these claims have not been amended in the manner discussed above for Claim 1, it is submitted that one of ordinary skill would have understood that these claims recite features of a discrete transistor device. It is submitted that one of ordinary skill would understand that a "metal-oxide-semiconductor device' that has a "length and a width", "first and second source/drain regions" and a "gate" *is* a MOS transistor device. As discussed above, Kato does not disclose an isolation structure that isolates portions of the first source/drain region and second source/drain region of the same transistor

device. Therefore, it is submitted that for these additional reasons, Claims 14 and 21 are not anticipated by Kato and that these claims and the claims that depend therefrom are allowable over Kato.

Accordingly, reconsideration and withdrawal of the rejection of these claims are respectfully requested.

B. Rejection under 35 U.S.C. §103

The Action rejects Claims 3-5, 8-12, 15-16, 19-20 and 23 as being obvious from Kato in view of several other references. These claims depend from independent Claims 1, 14 and 21. As set forth above, these claims are allowable for at least the reasons argued above for independent Claims 1, 14 and 21.

Reconsideration and withdrawal of the rejections of these claims are respectfully requested.

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IV. Conclusion

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

Dated: 9/11/06

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EXHIBIT